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Nozuyama

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[54] **DATA TRANSFER BUS INCLUDING DIVISIONAL BUSES CONNECTABLE BY BUS SWITCH CIRCUIT**

[75] Inventor: **Yasuyuki Nozuyama**, Tokyo, Japan

[73] Assignee: **Kabushiki Kaisha Toshiba**, Kawasaki, Japan

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[30] **Foreign Application Priority Data**

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[51] **Int. Cl.^{6}** **G06F 13/00**

[52] **U.S. Cl.** **395/311**; 395/280; 395/750.01; 395/311; 395/306; 395/307; 395/308

[58] **Field of Search** 395/280, 550, 395/800, 311, 307, 306, 308; 365/205; 364/200; 370/60

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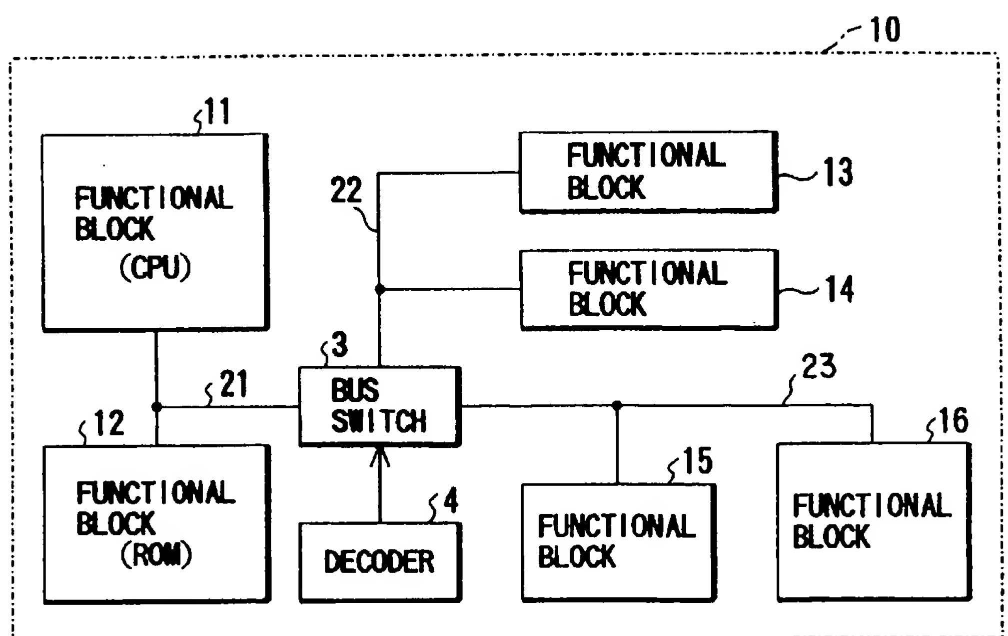
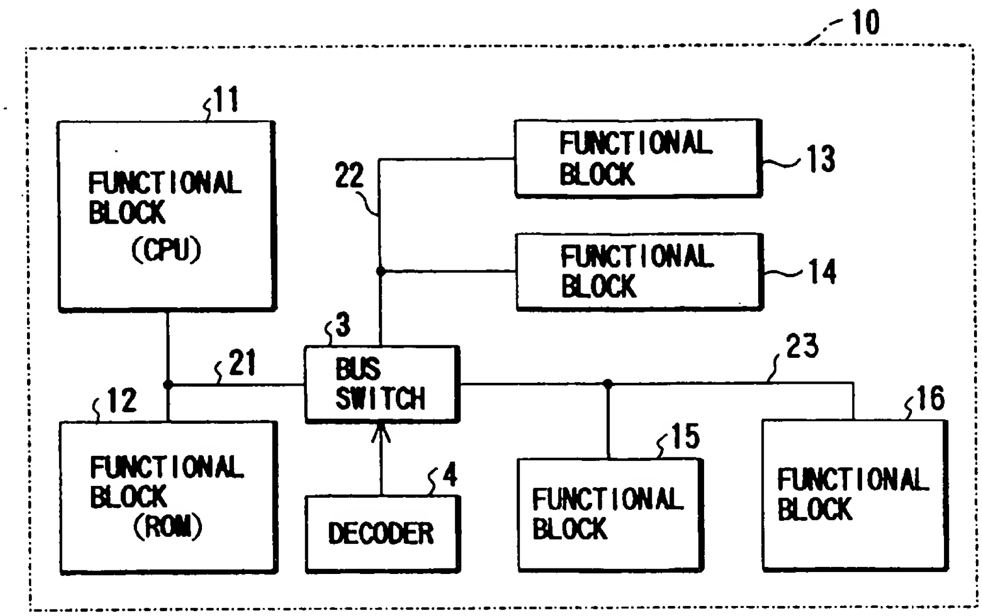
Primary Examiner—Thomas C. Lee
Assistant Examiner—Eric S. Thlang
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

[57] **ABSTRACT**

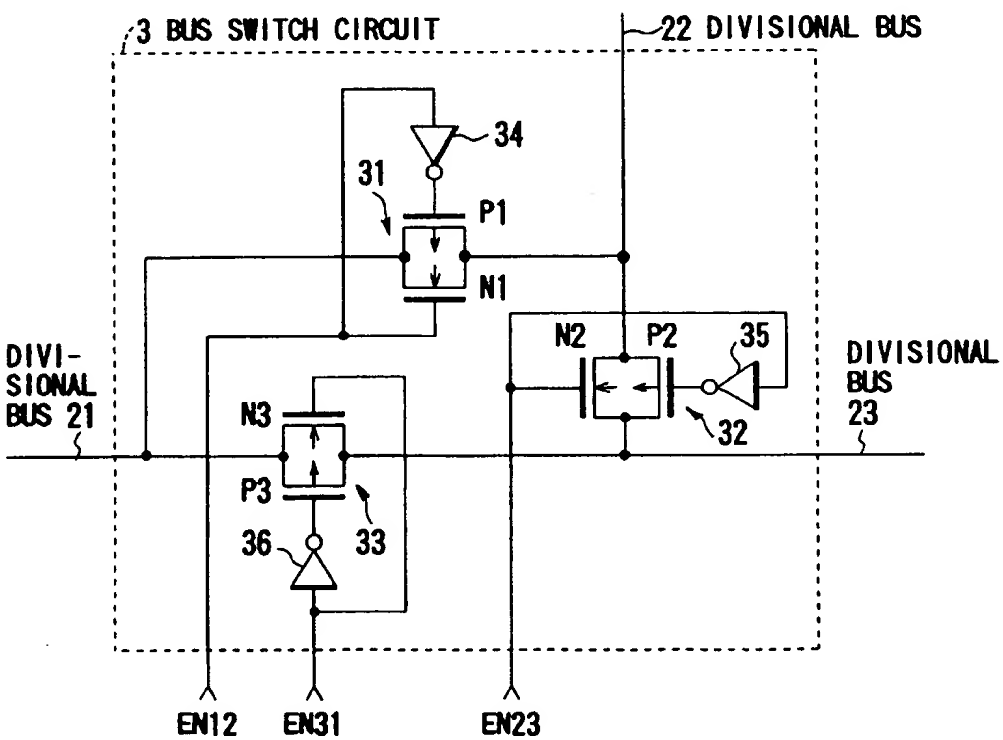
In the low power consumption data transfer bus of the present invention, the mode of division of a bus is associated with a specific layout on an actual LSI chip or an actual LSI-mounted board, and access frequency between functional blocks connected to the bus and therefore the effect of the bus division can be obtained to the maximum degree for the object of achievement of the low power consumption. Further, the operation speed of the bus (that is, data transfer speed) can be improved as compared to the case where the bus is not divided. The data transfer bus includes a bus switch circuit connected so that one data transfer bus provided between a plurality of functional blocks within an LSI is divided into three or more divisional buses, and a decoder circuit for decoding an order signal which requires two of the plurality of divisional buses during an operation of the data transfer bus, and controlling the bus switch circuit so that only the two divisional buses are connected to each other in reply to a decode output.

10 Claims, 3 Drawing Sheets

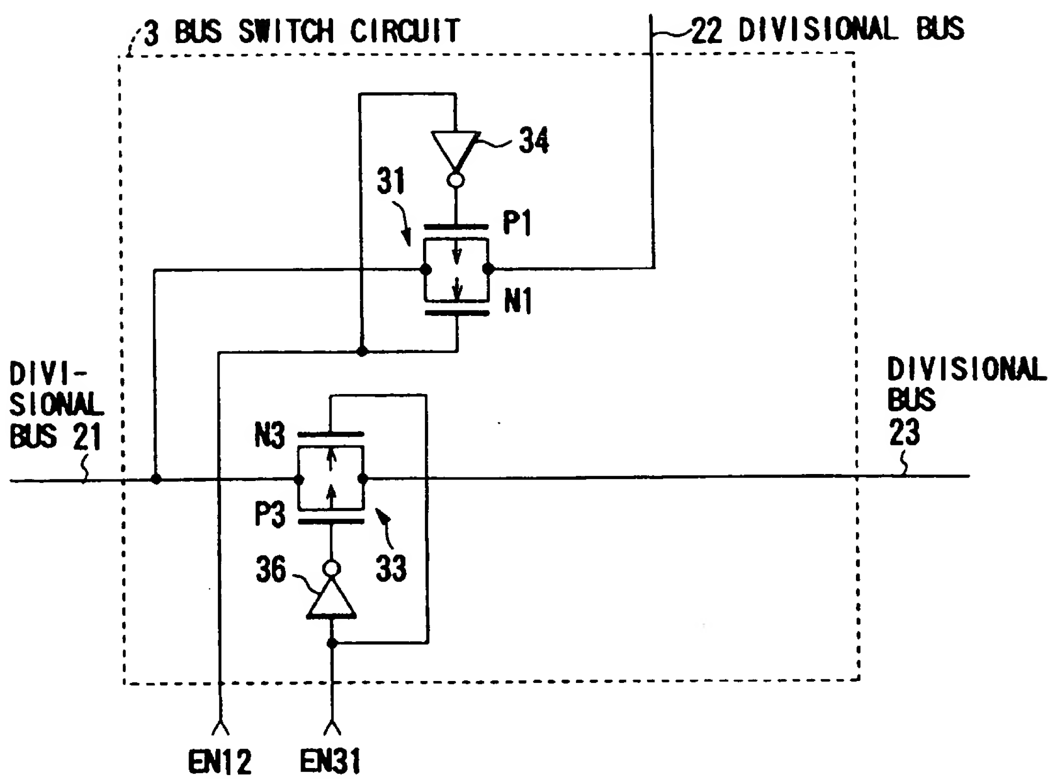



10
11
FUNCTIONAL BLOCK (CPU)
22
FUNCTIONAL BLOCK
13
FUNCTIONAL BLOCK
14
3
BUS SWITCH
21
23
12
FUNCTIONAL BLOCK (ROM)
4
DECODER
15
FUNCTIONAL BLOCK
16
FUNCTIONAL BLOCK

F I G. 1


3 BUS SWITCH CIRCUIT
22 DIVISIONAL BUS
34
31
P1
N1
N2
P2
35
DIVI-SIONAL BUS 21
DIVISIONAL BUS 23
N3
32
P3
36
33
EN12
EN31
EN23

F I G. 2A


3 BUS SWITCH CIRCUIT
22 DIVISIONAL BUS
34
31
P1
N1
DIVI-
SIONAL
BUS 21
N3
P3
36
33
DIVISIONAL
BUS
23
EN12
EN31

F I G. 2B

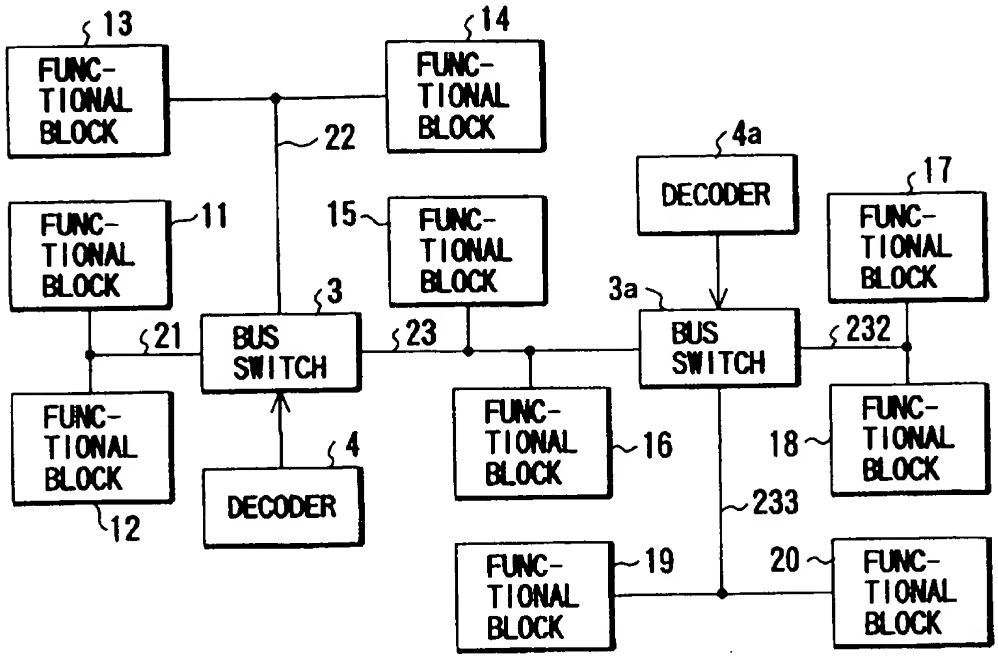

13
FUNC-TIONAL BLOCK
14
FUNC-TIONAL BLOCK
22
4a
DECODER
17
FUNC-TIONAL BLOCK
11
FUNC-TIONAL BLOCK
15
FUNC-TIONAL BLOCK
3
3a
21
BUS SWITCH
23
BUS SWITCH
232
FUNC-TIONAL BLOCK
12
4
DECODER
FUNC-TIONAL BLOCK
16
18
FUNC-TIONAL BLOCK
233
FUNC-TIONAL BLOCK
19
20
FUNC-TIONAL BLOCK

FIG. 3

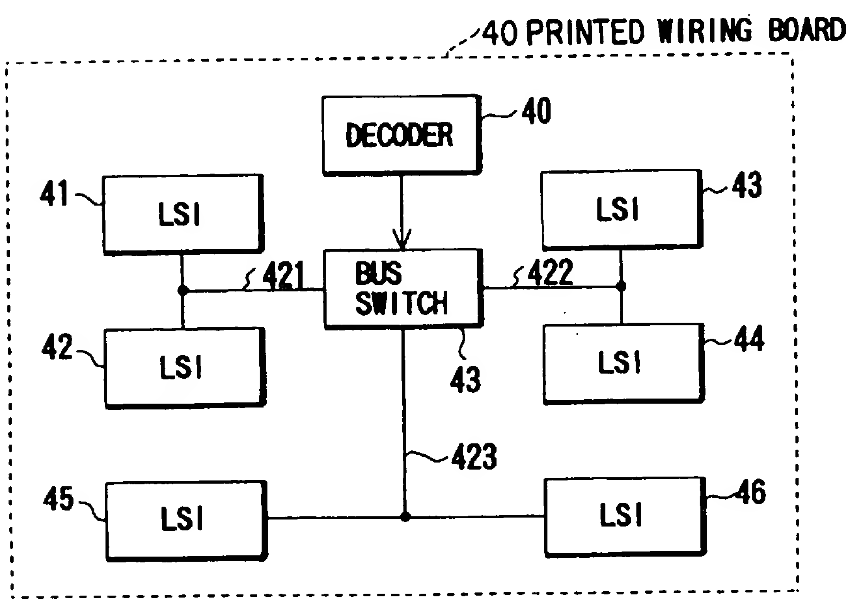

40 PRINTED WIRING BOARD
DECODER
40
41
LSI
43
LSI
421
BUS SWITCH
422
42
LSI
43
LSI
44
423
45
LSI
LSI
46

FIG. 4

DATA TRANSFER BUS INCLUDING DIVISIONAL BUSES CONNECTABLE BY BUS SWITCH CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a data transfer bus provided between a plurality of functional blocks inside an LSI such as a logic LSI (large-scale integrated circuit) or a VLSI (Very large-scale integrated circuit), or between a plurality of LSIs, and more specifically, to a low power consumption data transfer bus, to which a low power consumption technique was applied, for example, such a data transfer bus that is used in a micro-processor, a micro-controller or the like.

2. Description of the Related Art

Recently, the introduction of an LSI to a portable device is becoming very popular, and at the same time, there has been a problem of heat generation of an LSI, particularly, of a high performance type. Under these circumstances, there is an increasing demand for the development of an LSI or a VLSI of a low power consumption type.

An example of effective techniques of achieving a low power consumption is to decrease the power-supply voltage. In general, the power consumption of an LSI or the like is proportional to a square of the power-supply voltage. Therefore, for example, if the power-supply voltage is changed from 5V, which is most widely used at present time, to 3V, which is recently becoming popular, the power consumption decreases to 36% by itself.

However, if the competition between LSI vendors is taken into consideration, the lowering of the power-supply voltage is only the first step of the low power consumption. In order to meet the demand for the low power consumption, all of the levels of design, from the architecture, functions, circuit technique, to the processing technique, must be satisfied. At each level, effective measurements are, for example, to avoid operating a circuit when it is not necessary (to avoid wasting currents) and to avoid an excessive driving force (proportional to the size of a transistor) for the performance regarding the operation speed.

Generally, an LSI of a micro-processor, a micro-controller or the like, has a bus capable of transferring data between a plurality of functional blocks. The bus is connected to a number of functional blocks, and in many cases, drawn around in a wide area inside an LSI chip. Thus, the lowering of the power consumption of the bus greatly contributes to the achievement of the low power consumption of the LSI as a whole.

A conventional example of the low power consumption technique for a bus is a bus dividing method. In this method, one bus is divided into sections by a bus switch circuit, and the bus is operated only when it is needed. As a result, the average load capacitance driven can be decreased, and the power consumption can be lowered.

However, the mode of the above-described division of the bus is not considered in connection with a specific layout on an LSI chip, and therefore the achievement of the low power consumption is not completely realized. As the worst case, it is necessary to drive all the load on the bus. In this case, the load components situated on another side of the bus switch circuit as viewed from the buffer to drive the load, have to be driven via the bus switch circuit, and therefore the operation speed (data transfer speed) of the bus is decreased as compared to the case where the bus is not divided.

SUMMARY OF THE INVENTION

As described above, according to the conventional data transfer bus, the mode of the division of the bus is not considered in connection with a specific layout on an LSI chip, and therefore the achievement of the low power consumption is not completely realized, and the operation speed (data transfer speed) of the bus is decreased as compared to the case where the bus is not divided.

The present invention has been proposed as a solution to the above-described problems, and is achieved by associating the mode of the bus division with a specific layer on an actual LSI chip or an LSI-mounted board. The object of the present invention is to provide a low power consumption data transfer bus, in which the effect of the bus division can be induced to the maximum degree so as to achieve the low power consumption, and the operation speed (data transfer speed) of the bus can be improved as compared to the case where the bus is not divided.

A low power consumption data transfer bus according to the first aspect of the present invention, includes a bus switch circuit connected so that one data transfer bus provided between a plurality of functional blocks inside an LSI is divided into 3 or more divisional buses. The data transfer bus further comprises a decoder circuit which decodes a control signal which requires two of the three or more divisional buses during an operation, and controls the bus switch circuit so that only the two divisional buses are connected to each other in reply to a decode output.

A low power consumption data transfer bus according to the second aspect of the invention, includes a bus switch circuit connected so that one data transfer bus provided on a print wiring board on which a plurality of LSIs are mounted, and between the plurality of LSIs is divided into 3 or more divisional buses at one place. The data transfer bus further comprises a decoder circuit which decodes a control signal which requires two of the three or more divisional buses during an operation, and controls the bus switch circuit so that only the two divisional buses are connected to each other in reply to a decode output.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention and, together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIG. **1** is a block diagram illustrating a low power consumption data transfer bus according to the first embodiment of the first aspect of the present invention;

FIG. **2A** is a circuit diagram illustrating a specific example of a 1-bit section of the bus switch circuit shown in FIG. **1**;

FIG. **2B** is a circuit diagram which is the same as FIG. **2A** when there is no access between the divisional bus **22** and **23**.

FIG. **3** is a block diagram illustrating a low power consumption data transfer bus according to the second embodiment of the first aspect of the present invention; and

FIG. **4** is a block diagram illustrating a low power consumption data transfer bus according to the second aspect of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will now be described in detail with reference to accompanying drawings.

FIG. 1 is a circuit diagram showing a low power consumption data transfer bus of an LSI according to the first embodiment of the present invention.

As can be seen in FIG. 1, on an LSI **10** (for example, a micro-controller), a plurality of function blocks **11** to **16** such as a CPU, ROM, RAM and I/O interface, are provided.

Further, a bus switch circuit **3** is provided, which is connected such that one data transfer bus provided between the plurality of function blocks **11** to **16** within the LSI is divided into 3 or more divisional buses **21** to **23** (in this embodiment, 3).

Further, a decoder circuit **4** is provided, which serves to a control signal (supplied from the CPU, for example) which requires 2 of the divisional buses **21** to **23** in the operation of the data transfer bus, and control the bus switch circuit such that only the two of the divisional buses are connected to each other at one place on the basis of a decoded output.

It should be noted that in this embodiment, the number of the bus switch circuit **3** and the decoder circuit **4** is 1, respectively, and the bus switch circuit **3** is located at a predetermined region on the LSI chip **10**.

Loads on the divisional buses **21** to **23** are arranged asymmetrically. Of the plurality of functional blocks **11** to **16**, a pair of functional blocks which have the highest average access frequency with respect to the data transfer bus, (for example, CPU and ROM) are connected to one of the divisional buses **21** to **23**, which has the smallest load (**21** in this embodiment).

In other words, in FIG. **1**, the divisional bus **21**, to which a pair of functional blocks which have the highest average access frequency are connected, is constituted so that the load thereon is the smallest under the restriction of the floor layout of the plurality of functional blocks **11** to **16** on the LSI chip **10**.

It should be noted that a load on a divisional bus includes a load component due to wiring, a load component of an output buffer of the functional block for outputting data to the divisional bus, and a load component of an input buffer of the functional block for receiving date from the divisional bus.

The access frequency to a functional block connected to a divisional bus is defined in the unit of a pair of a functional block for outputting data to the divisional bus and a functional block for receiving data from the divisional bus, and the data of the access frequency can be obtained by operating the LSI in simulation.

In the structure shown in FIG. **1**, the entire power consumption P is proportional to:

$$S=\Sigma F_i \cdot L_i$$

where F_i represents the access frequency of the i-th number of the divisional bus, and L_i represents the load thereon. With this relationship, the minimization of the above $\Sigma F_i \cdot L_i$ will now be considered.

Supposing that $1=\Sigma F_i$ and the access frequency of a divisional bus of a smaller number is higher than the access frequency of a divisional bus of a larger number, the following relationship is established:

$$F_i > F_{i+1}$$

Next, a procedure of carrying out the division of a bus which is close to the optimal for achieving the low power consumption, will now be described.

First, a pair of functional blocks (the first pair of functional blocks) having the maximum access frequency (the first access frequency) $f_i(=F_i)$ are connected to a first divisional bus **21**. Then, in consideration of the layout of the first functional blocks on the LSI chip **10**, a layout is made so that the load on the first divisional bus **21** becomes minimum.

Next, whether a pair of functional blocks (the second pair of functional blocks) having the second maximum access frequency (the second access frequency) f_2 to the maximum access frequency should be connected to the first divisional bus **21**, or to a second divisional bus **22**, is considered. It should be noted that, if the above two types (the first pair and the second pair) of functional blocks are substantially independent from each other, it is clear by intuitively that the the second pair of functional blocks should be connected to the second divisional bus.

The case where one of the second pair of functional blocks (for example, CPU) is the same as either one of the first pair of functional blocks, will now be considered. In the relationships provided below, F_1 represents the access frequency to the first divisional bus **21** in the case where the presence of the second pair of functional blocks is not considered (but an area in which it is laid out is maintained), L_1 represents the load thereon, F_2 represents the access frequency to the second divisional bus **22**, L_2 represents the load thereon, f represents the access frequency to another block of the second pair of functional blocks, and l_1 and l_2 represents the load appended to the first divisional bus **21** and the second divisional bus, respectively, when another block is connected to the respective bus.

The amount which is proportional to the power consumption which increases in the case where the second pair of functional blocks are connected to the first divisional bus **21** is given by:

$$S_1=(F_1+f)\cdot(L_1+l_1)+F_2\cdot(L_1+L_2)$$

In contrast, the amount which is proportional to the power consumption which increases in the case where the second pair of functional blocks are connected to the second divisional bus **22** is given by:

$$S_2=F_1\cdot L_1+(F_2+f)\cdot(L_1+L_2+l_2)$$

Therefore, the condition for that the power consumption becomes lower if the second pair of functional blocks are connected to the second divisional bus **22**, is given by:

$$S_2-S_1<0$$

That is, $(F_2+f)\cdot l_2+f\cdot L_2-(F_1+f)\cdot l_1<0$ $f\cdot(L_2+l_2l_1)<F_1\cdot l_1-F_2\cdot l_2$

It is clear that if the above condition is satisfied, the case where the second pair of functional blocks are connected to the second divisional bus **22** is more effective in terms of the power consumption.

As the procedure similar to the above is repeated, a bus having a closely minimum power consumption as a whole can be constituted.

It should be noted that the procedure is one of several methods for constituting a bus having a closely minimum power consumption as a whole.

Regarding actual micro-computers or the like, in many cases, there is a clear contrast between a functional block pair having a high access frequency and a functional block pair not having such a frequency. Therefore, if the designer of an LSI designs it by trial and error following the above-described procedure, while considering the layout on the LSI chip **10**, it is expected that the designer can achieve a closely minimum power consumption without much difficulty.

However, in the case where there is not a significant difference between functional block pairs in the access frequency, it is expected that the minimum solution for the power consumption cannot be easily found out manually. In order to obtain the minimum solution in a restrict sense, it is necessary to use a mathematical technique for obtaining the minimum solution. In this case, there are an excessive number of parameters to be optimized, and therefore in some cases, the solution becomes a quasi-minimum. In order to avoid this, it is preferable that a method by which a solution close to the minimum can be easily found, such as the simulated annealing method, should be utilized.

Further, if there is a restriction regarding the operation speed of a bus, such a restriction must also be taken into consideration. However, the bus switch circuit **3** is positioned in one place in order to satisfy the condition by which only the target two types of divisional busses are operated at the same time as described before, and therefore the restriction can be expressed in a simple form. That is, for all of L_i and L_j (i and j are different from each other), the designing should be conducted so that the relationship: L_i+L_j<the upper limit of the load which satisfies the operation speed of the bus, is satisfied.

Thus, the low power consumption data transfer bus of an LSI, according to the first embodiment, the mode of the bus division is associated with a specific layout on an actual LSI chip **10**. With this structure, the effect of the bus division can be obtained to the maximum degree for the achievement of the low power consumption, and the operation speed (data transfer speed) of the bus can be improved to a certain degree as compared to the case where the bus is not divided.

It is also a possibility that the present invention is used so as to control the power consumption substantially to a possible lower limit, while maintaining the operation speed (data transfer speed) of the bus substantially to a possible upper limit by the divisional bus mode of the present invention. In order to achieve this, pairs of functional blocks which require high bus operating speeds are registered in advance. Then, while executing the above-described flow for achieving the low power consumption, the maximum bus load which satisfy the operation speed is obtained for each of the case where data signal crosses the bus switch circuit, and the case where it does not. Then, each time an appropriate functional block under the condition of the operation speed appears, this functional block should be connected to a predetermined divisional bus with a priority to functional blocks determined in terms of the demand for the achievement of the low power consumption. At any rate, in order to increase the operation speed, it is only natural that a pair of functional blocks which require the most restricted bus operation speed, should be connected to a divisional bus having the smallest load capacity. Note that the above description was made in consideration of that the data transfer which crosses the bus switch circuit generally requires a more time that the case where the transfer does not cross the circuit. More simply stating, it is possible that if a pair of functional blocks which require a shorter data transfer time, are connected to the same divisional bus, a similar effect can be obtained.

FIG. 2A shows a specific example of a 1-bit portion of the bus switch circuit **3** shown in FIG. **1**. As can be seen in FIG. **2A**, a first CMOS switch circuit **31** is connected between a first divisional bus **21** and a second divisional bus **22**, a second CMOS switch circuit **32** is connected between the second divisional bus **22** and a third divisional bus **23**, and a third CMOS switch circuit **33** is connected between the third divisional bus **23** and the first divisional bus **21**.

In the first CMOS switch circuit **31**, a transmission gate made of a first PMOS transistor **P1** and a first NMOS transistor **N1**, is used, in the second CMOS switch circuit **32**, a transmission gate made of a second PMOS transistor **P2** and a second NMOS transistor **N2**, is used, and in the third CMOS switch circuit **33**, a transmission gate made of a third PMOS transistor **P3** and a third NMOS transistor **N3**, is used.

A first control signal **EN12** used for controlling the connection of the first divisional bus **21** and the second divisional bus **22**, is supplied to the gate of the first NMOS transistor **N1**, and at the same time, after being inverted by a first inverter circuit **34**, is supplied to the gate of the first PMOS transistor **P1**.

A second control signal **EN23** used for controlling the connection of the second divisional bus **22** and the third divisional bus **23**, is supplied to the gate of the second NMOS transistor **N2**, and at the same time, after being inverted by a second inverter circuit **35**, is supplied to the gate of the second PMOS transistor **P2**.

A third control signal **EN31** used for controlling the connection of the third divisional bus **23** and the third divisional bus **21**, is supplied to the gate of the third NMOS transistor **N3**, and at the same time, after being inverted by a third inverter circuit **36**, is supplied to the gate of the third PMOS transistor **P3**.

Each of the above control signals **EN12** to **EN31** is set in an active state (level "H" in this embodiment) when corresponding two divisional buses are to be connected, and otherwise set in an inactive state (level "L" in this embodiment).

It should be noted that each of the CMOS switch circuits **31** to **33** is not limited to a transmission gate as described above, but can be remodeled into some other structure.

It should be also noted that, as depicted in FIG. **2B**, the switch circuit is not necessary between a pair of divisional busses functional blocks connected to one (**22**) of which have no access between those connected to another (**23**).

FIG. **3** shows a low power consumption data transfer bus of an LSI, according to the second embodiment of the first aspect of the present invention.

The low power consumption data transfer bus shown in FIG. **3** is similar to the data transfer bus shown in FIG. **1** except for the following points. That is, a part of the divisional buses (denoted by reference numeral **23** in this embodiment) is connected so that the part is further divided into three or more divisional buses **232** to **233** by a second bus switch circuit **3*a***, and functional blocks **17** to **20** are connected to the newly divided buses. Further, a second decoder circuit **4*a*** which corresponds to the second bus switch circuit **3*a*** is provided, and the bus switch circuits **3** and **3*a*** are arranged away from each other on the chip of the LSI. Structural elements shown in FIG. **3**, which are similar to those in FIG. **3** are designated by the same reference numerals.

According to the second embodiment, basically a similar effect to that of the first embodiment can be obtained; however the power consumption increases by the degree corresponding to an increase in the number of elements

used. In the case where the pattern area is enlarged if the bus switch circuit is arranged at one place as in the first embodiment, due to the layout on the LSI chip, the increase in the pattern area and the increase in the power consumption trade off with each other. In the case, the second embodiment is recommended to be employed.

FIG. 4 shows a low power consumption data transfer bus on an LSI-mounted board, according to an embodiment of the second aspect of the present invention.

The low power consumption data transfer bus shown in FIG. 4 includes a bus switch circuit 43 connected so that one data transfer bus provided between a plurality of LSIs 41 to 46 mounted on a printed wiring board (substrate) 40 is divided into three or more divisional buses. The data transfer bus further includes a decoder circuit 44 for decoding an order signal which requires two of the divisional buses in the operation of the data transfer bus, and for controlling the bus switch circuit so that only the two of the divisional buses are connected to each other in reply to the decode output.

With the embodiment of the second aspect of the invention, a similar effect to that of the first embodiment of the first aspect of the invention can be obtained by a similar operation.

As described above, with the low power consumption data transfer bus according to the present invention, the mode of division of a bus is associated with a specific layout on an actual LSI chip or an actual LSI-mounted board, and access frequency between functional blocks connected to the bus and therefore the effect of the bus division can be obtained to the maximum degree for the object of achievement of the low power consumption. Further the operation speed of the bus (that is, data transfer speed) can be improved as compared to the case where the bus is not divided.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, and representative devices shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

1. A low power consumption data transfer bus comprising:

an LSI;

a plurality of functional blocks within said LSI;

a data transfer bus provided between said plurality of functional blocks;

three or more divisional buses obtained by dividing said data transfer bus;

a bus switch circuit for connecting said plurality of divisional buses to each other; and

a decoder circuit for decoding an order signal which requires two of said plurality of divisional buses during an operation of said data transfer bus, and controlling said bus switch circuit so that only said two divisional buses are connected to each other in reply to a decode output,

wherein said bus switch circuit is positioned in a predetermined section on a chip of said LSI and loads on said divisional buses are asymmetrical.

2. A low power consumption data transfer bus according to claim 1, wherein, of said plurality of functional blocks, a pair of functional blocks having a highest average access frequency with respect to the data transfer bus are connected to a divisional bus having a lightest load of said plurality of divisional buses.

3. A low power consumption data transfer bus according to claim 1, wherein said plurality of functional blocks are registered in the order of a data transfer time which is allowed to be shorter;

a maximum load which satisfies a predetermined data transfer time is obtained in both a case where data crosses the bus switch circuit, and a case where data does not cross the bus switch circuit;

a procedure that a pair of functional blocks having a highest average access frequency with respect to the data transfer bus, of said plurality of functional blocks, are connected to a divisional bus having a lightest load of said plurality of divisional buses, is executed; and

each time a functional block conforming to a condition of said data transfer time appears, said functional block is connected to a predetermined divisional bus prior to a functional block determined due to a power-saving requirement.

4. A low power consumption data transfer bus according to claim 1, wherein, of said plurality of functional blocks, a pair of functional blocks which require a shortest data transfer time are connected to a divisional bus having a lightest load of said plurality of divisional buses.

5. A low power consumption data transfer bus comprising:

an LSI;

a plurality of functional blocks within said LSI;

a data transfer bus provided between said plurality of functional blocks;

three or more divisional buses obtained by dividing said data transfer bus;

a bus switch circuit for connecting said plurality of divisional buses to each other;

a decoder circuit for decoding an order signal which requires two of said plurality of divisional buses during an operation of said data transfer bus, and controlling said bus switch circuit so that only said two divisional buses are connected to each other in reply to a decode output; and

a second bus switch circuit connected so that a part of said divisional buses is further divided into three or more divisional buses,

wherein said bus switch circuit and said second bus switch circuit are arranged to be away from each other in the chip of said LSI.

6. A low power consumption data transfer bus comprising:

a printed circuit board;

a plurality of LSIs mounted on said printed circuit board;

a data transfer bus provided between said plurality of LSIs;

a plurality of divisional buses obtained by dividing said data transfer bus;

a bus switch circuit for connecting said plurality of divisional buses to each other; and

a decoder circuit for decoding an order signal which requires two of said plurality of divisional buses during an operation of said data transfer bus, and controlling said bus switch circuit so that only said two divisional buses are connected to each other in reply to a decode output,

wherein said bus switch circuit is positioned in a predetermined section on said printed circuit board and loads on said divisional buses are asymmetrical.

7. A low power consumption data transfer bus according to claim 6, wherein, of said plurality of LSIs, a pair of LSIs having a highest average access frequency with respect to the data transfer bus are connected to a divisional bus having a lightest load of said plurality of divisional buses.

8. A low power consumption data transfer bus according to claim 6, wherein said plurality of LSIs are registered in the order of a data transfer time which is allowed to be shorter;

a maximum load which satisfies a predetermined data transfer time is obtained in both a case where data crosses the bus switch circuit, and a case where data does not cross the bus switch circuit;

a procedure that a pair of LSIs having a highest average access frequency with respect to the data transfer bus, of said plurality of LSIs, are connected to a divisional bus having a lightest load of said plurality of divisional buses, is executed; and

each time an LSI conforming to a condition of said data transfer time appears, said LSI is connected to a predetermined divisional bus prior to an LSI determined due to a power-saving requirement.

9. A low power consumption data transfer bus according to claim 6, wherein, of said plurality of LSIs, a pair of LSIs which require a shortest data transfer time are connected to a divisional bus having a lightest load of said plurality of divisional buses.

10. A low power consumption data transfer bus comprising:

a printed circuit board;

a plurality of LSIs mounted on said printed circuit board;

a data transfer bus provided between said plurality of LSIs;

a plurality of divisional buses obtained by dividing said data transfer bus;

a bus switch circuit for connecting said plurality of divisional buses to each other;

a decoder circuit for decoding an order signal which requires two of said plurality of divisional buses during an operation of said data transfer bus, and controlling said bus switch circuit so that only said two divisional buses are connected to each other in reply to a decode output; and

a second bus switch circuit connected so that a part of said divisional buses is further divided into three or more divisional buses,

wherein said bus switch circuit and said second bus switch circuit are arranged to be away from each other in the printed circuit board.

* * * * *

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(54) **COMBINED LOW SPEED AND HIGH SPEED DATA BUS**

(75) Inventors: **Jeppa Grosshög**, Staffanstorp (SE); **Lars Novak**, Bjärred (SE)

(73) Assignee: **Telefonaktiebolaget LM Ericsson (publ)** (SE)

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(52) **U.S. Cl.** **710/107**; 710/105; 710/60
(58) **Field of Search** 710/105–106, 710/60–61, 33–35, 107, 110; 709/233, 234

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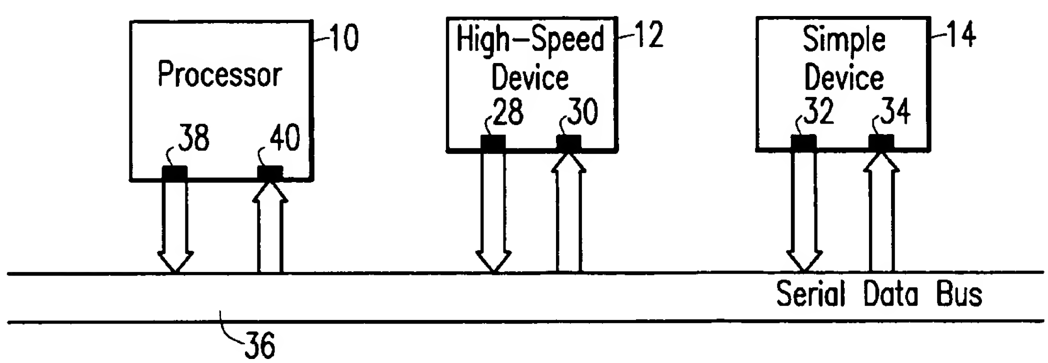
Primary Examiner—Peter Wong
Assistant Examiner—Raymond N Phan
(74) *Attorney, Agent, or Firm*—Jenkens & Gilchrist

(57) **ABSTRACT**

A method and system for communicating at least two data transfers on a common bus. Data is communicated between a simple device and a system processor or system connector via the common bus at a low data rate, and data is communicated between a more complex device and the system processor or system connector via the common bus at a high data rate. Low data rate communications are conducted by selectively varying the voltage level on the common bus at least between a low voltage range and a high voltage range, wherein the low voltage range represents a first data value and the high voltage range represents a second data value. High data rate communications can be conducted, simultaneous with the low data rate communications, by selectively varying the voltage level on the common bus at least between two voltage sub-levels within the low voltage range and between two voltage sub-levels within the high voltage range.

23 Claims, 2 Drawing Sheets



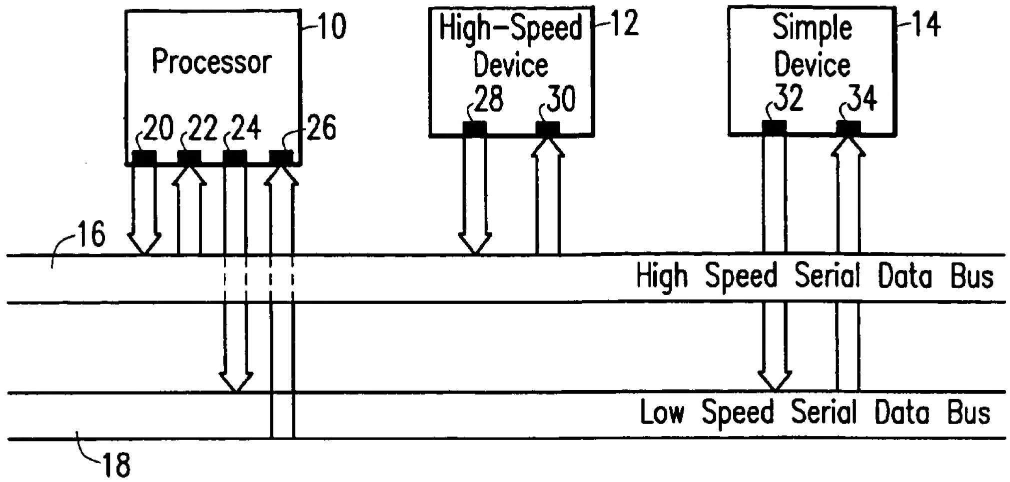


FIG. 1
(PRIOR ART)

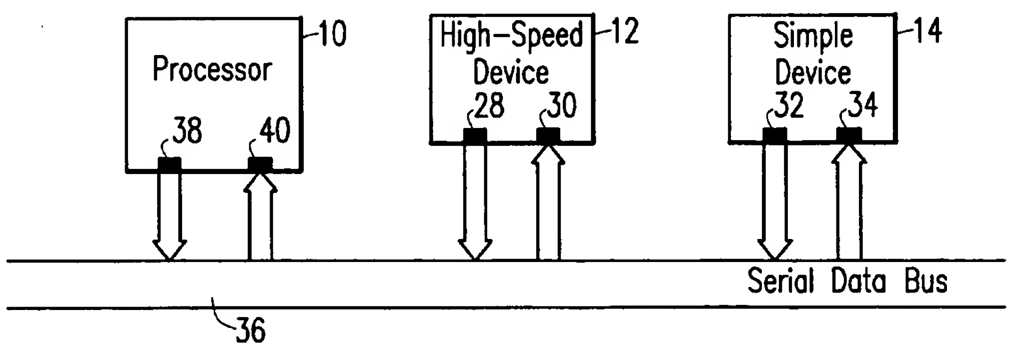


FIG. 2

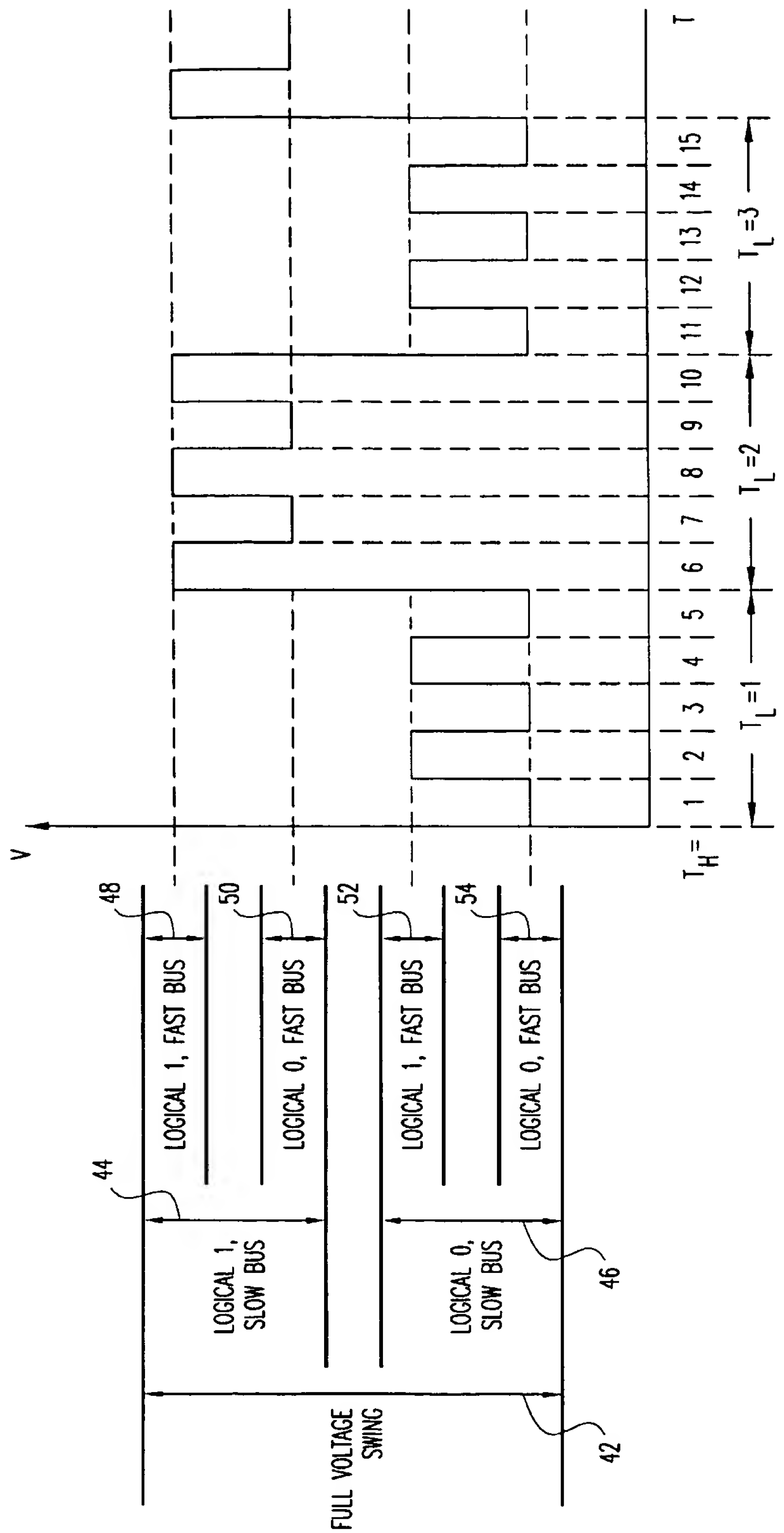

FULL VOLTAGE SWING
42
LOGICAL 1, SLOW BUS
44
LOGICAL 0, SLOW BUS
46
LOGICAL 1, FAST BUS
48
LOGICAL 0, FAST BUS
50
LOGICAL 1, FAST BUS
52
LOGICAL 0, FAST BUS
54
V
T
T_H=
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
T_L=1
T_L=2
T_L=3

FIG. 3

COMBINED LOW SPEED AND HIGH SPEED DATA BUS

BACKGROUND OF THE INVENTION

1. Technical Field of the Invention

The present invention relates in general to a system and method for communicating data, and in particular for simultaneously communicating data between multiple devices on a shared data bus.

2. Description of Related Art

Different electronics devices communicate data at different rates. Generally, the data rate for a particular device is dependent upon how advanced the device is and upon the rate of data exchange that is required for proper operation of the device. For example, low-cost electronics accessories typically operate at a low data rate and use a simple electrical interface. More advanced accessories, on the other hand, frequently require the use of electrical data buses that can support high data rates.

Many products and systems that incorporate electronic accessories, such as cellular telephones, include a number of interconnected devices, which can have varying levels of complexity. Some of the more complex devices must operate at high data rates while many of the simpler devices are incapable of operating at a high data rate. As a result, such systems or products typically require two or more electrical data buses to support communications with the various devices of the particular system or product, increasing space requirements and cost. The use of multiple data buses also requires a greater number of connector pins on system connectors and processors that control the system or product, which also takes up more space and adds expense.

There is a need, therefore, for a system and method for communicating data to and from both high-speed devices and low-speed devices using a common electrical bus. Such a system and method would reduce the space and the number of connector pins required to interconnect multiple devices having the same or differing data rates. In addition, such a system and method would preferably permit the simultaneous use of the common electrical data bus for both high-speed and low-speed data transfers.

SUMMARY OF THE INVENTION

The present invention comprises a method and system for communicating at least two data transfers on a shared data bus. The system includes a simple electronic device that communicates via the shared data bus at a low data rate and a high-speed electronic device that communicates via the shared data bus at a high data rate. Alternatively, two devices can transmit data via the data bus at the same time using the same data rate. Generally, the shared data bus is also connected to a system processor, system connector, and/or other high-speed or low-speed devices.

Communications at the low data rate are conducted by varying a voltage level on the shared data bus within the full voltage swing of the shared data bus. The full voltage swing is divided into at least a low voltage range and a separate high voltage range. A voltage level on the shared data bus that is within the low voltage range represents a first data value, such as a binary value of zero, and a voltage level on the shared data bus that is within the high voltage range represents a second data value, such as a binary value of one. Thus, devices can communicate via the shared data bus at the low data rate by selectively varying the voltage level between at least the low voltage range and the high voltage range.

At the same time as communications at the low data rate are ongoing, communications at the high data rate can also be conducted by varying the voltage level within either the low voltage range or the high voltage range, depending on which data value is currently being transmitted at the low data rate. Accordingly, the low voltage range and the high voltage range are each divided into sub-levels or sub-ranges. Thus, when a device communicating at the low data rate is transmitting the first data value (i.e., within the low voltage range), a high-speed device can simultaneously transmit data at the high data rate by varying the voltage level between sub-levels within the low voltage range. Similarly, when a device communicating at the low data rate is transmitting the second data value (i.e., within the high voltage range), a high-speed device can simultaneously transmit data at the high data rate by varying the voltage level between sub-levels within the high voltage range.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, reference is made to the following detailed description taken in conjunction with the accompanying drawings wherein:

FIG. **1** is an arrangement of interconnected devices that operate at different rates of data transfer, as can be found in existing products and systems;

FIG. **2** is an arrangement of interconnected devices that operate at different rates of data transfer and that use a shared data bus, in accordance with the present invention; and

FIG. **3** is a graph illustrating an exemplary data transmission on a shared data bus using both a high data rate and a low data rate in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference is now made to the Drawings wherein like reference characters denote like or similar parts throughout the various Figures. Referring now to FIG. **1**, there is illustrated an arrangement of interconnected devices that operate at different rates of data transfer, as can be found in existing products and systems. The arrangement includes a high-speed device **12** that transmits and receives data over a high speed serial data bus **16** at a high data rate. The high-speed device **12** communicates with a processor **10** or system connector (not shown) via the high speed serial data bus **16**. In addition, the high-speed device **12** can communicate via the high speed serial data bus **16** with other devices (not shown) that are capable of operating at a high data rate.

The arrangement also includes a simple device **14** that is not capable of operating at a high data rate. Instead, the simple device **14** requires a separate low speed serial data bus **18** to transmit and receive data. The simple device **14** communicates with the processor **10** via the low speed serial data bus **18** and can also communicate, again via the low speed serial data bus **18**, with other devices (not shown) that are capable of transmitting and/or receiving information at a low data rate. Furthermore, the processor **10** can send information that is received from the simple device **14** to the high-speed device **12** by sending the received data at a faster rate over the high speed serial data bus **16**. Similarly, the processor **10** can also transform data received from the high speed device **12** for transmission to the simple device **14**.

Because it is desirable to have the capability to operate in a full duplex mode, wherein data can be simultaneously sent

and received over the high speed serial data bus 16 or the low speed serial data bus 18, the processor 10 (and any other devices capable of using both the high speed serial data bus 16 and the low speed serial data bus 18) must include two pins for each serial data bus 16 and 18. Thus, the processor 10 must include an output pin 20 for transmitting data over the high speed serial data bus 16 and an input pin 22 for receiving data from the high speed serial data bus 16. The high speed device 12 includes corresponding output and input pins 28 and 30 so that it too can support full duplex operation.

In addition, to support low speed data communications as well, the processor 10 must further include an output pin 24 for transmitting data over the low speed serial data bus 18 and an input pin 26 for receiving data from the low speed serial data bus 18. The low speed device 14 also includes corresponding output and input pins 32 and 34 for supporting full duplex operation. If one or more additional serial data buses having other rates of data exchange are also handled by the processor 10, then additional pairs of input and output pins might also be required for connecting the processor 10 to the additional data buses. The need for two separate data buses and for four connector pins on the processor 10 and other system connectors (not shown), however, increases the space requirements for, and increases the cost associated with, constructing a product or system that uses both high-speed and low-speed components.

Referring now to FIG. 2, however, there is illustrated an arrangement of interconnected devices that operate at different rates of data transfer and that use a shared data bus 36, in accordance with the present invention. In this arrangement, a high-speed device 12 and a low-speed device 14 are incorporated in an interconnected system or product using a shared data bus 36. As in the arrangement of FIG. 1, the invention permits full duplex operation because each device 10, 12, and 14 includes separate input and output connector pins. Because only one data bus 36 is used, however, the processor 10 (or other system connector) only requires one output connector pin 38 and one input connector pin 40 instead of the four connector pins used in the arrangement of FIG. 1.

Using the output connector pin 38, the processor 10 can transmit data via the shared data bus 36 at both a high data rate and a low data rate by using distinguishable, but overlapping, encoding methods, as described below. In particular, the data transmitted at a high data rate is superimposed on the data transmitted at a low data rate. Thus, the processor 10 can transmit data to the high-speed device 12 by sending the data at a high data rate from the output connector pin 38 onto the shared data bus 36. The high-speed device 12 then receives the transmitted data at its input connector pin 30. The processor 10 can also transmit data to the simple device 14 by sending the data at a low data rate from the same output connector pin 38 onto the-shared data bus 36. The simple device 14 then receives the transmitted data at its input connector pin 34.

Similarly, the processor 10 can receive data that is transmitted via the shared data bus 36 at both a high data rate and a low data rate using the input connector pin 40. In particular, the high-speed device 12 can send data at a high data rate from its output connector pin 28 and onto the shared data bus 36. The processor 10 receives the data transmitted from the high-speed device 12 at the processor's input connector pin 40. The simple device 14 can also transmit data to the processor 10 by sending the data at a low data rate from the simple device's output connector pin 32 onto the shared data bus 36. The processor 10 then receives the transmitted data at its input connector pin 40. Thus, data communications can be conducted using a single shared data bus 36 and shared input and output connector pins 38 and 40 at the system processor 10.

Referring now to FIG. 3, there is depicted a graph illustrating an exemplary data transmission using both a high data rate and a low data rate in accordance with the present invention. To transmit data communications on the shared data bus 36 (see FIG. 2), a transmitting device varies a voltage level on the shared data bus 36. The voltage is varied within a full voltage swing 42, which ranges, for example, between a minimum voltage of 0 V and a maximum of 100 mV. In such a system, a high voltage level typically represents a binary value of one, and a low voltage level represents a binary value of zero. Alternatively, a high voltage level can represent a binary value of zero, and a low voltage level can represent a binary value of one.

In accordance with the present invention, the full voltage swing 42 is used for transmitting data at the low data rate, but rather large variations in the voltage levels that represent the respective binary values of zero and one are permitted. In other words, a voltage level that is anywhere within a high voltage range 44 represents a logic value of one for purposes of transmitting data at the low data rate, and a voltage level that is anywhere within a low voltage range 46 represents a logic value of zero for purposes of transmitting data at the low data rate. Three full time slots (i.e., T_L=1, 2, and 3) for transmitting data at the low data rate are depicted in FIG. 3. Despite the relatively wide variation of voltage levels within each time slot T_L, the voltage level remains within one of the particular voltage ranges 44 and 46 for an entire time slot T_L and thus the transmitted data has a logical value of zero for the entire time slot T_L=1, a logical value of one for T_L=2, and a logical value of zero for T_L=3.

Although the data transmission is shown as oscillating between high and low voltages, the voltage level in actual use will not generally follow a set pattern but will depend upon the data value to be transmitted at each time slot T_L. In the preferred embodiment, as illustrated, data is transmitted as a binary code. Accordingly, only two different voltage ranges 44 and 46 are used. As an alternative, however, data can be encoded in more than two values per time slot T_L by dividing the full voltage swing 42 into greater numbers of voltage ranges, wherein each voltage range corresponds to a different value.

To transmit data at a high data rate, shorter time slots T_H are used. In addition, the high voltage range 44 that is used for low data rate transmissions is further divided into two voltage sub-ranges—a high sub-range 48 and a low sub-range 50. The high sub-range 48 of the high voltage range 44 represents a logic value of one for purposes of transmitting data at the high data rate, while the low sub-range 50 of the high voltage range 44 represents a logic value of zero for purposes of transmitting data at the high data rate. Similarly, the low voltage range 46 that is used for low data rate transmissions is also further divided into two voltage sub-ranges--a high sub-range 52 and a low sub-range 54. The high sub-range 52 of the low voltage range 46 represents a logic value of one for purposes of transmitting data at the high data rate, while the low sub-range 54 of the low voltage range 46 represents a logic value of zero for purposes of transmitting data at the high data rate. By varying the voltage levels on the shared data bus 36 between sub-ranges 48 and 50 or sub-ranges 52 and 54, depending on whether the low data rate transmission is high or low at a particular time, data can be transmitted over the shared data bus 36 at a high data rate at the same time as different data is being

transmitted over the shared data bus 36 at a low data rate. Data can, therefore, be transmitted at two different data rates simultaneously. Alternatively, instead of using entire sub-ranges, specific voltage levels within each of the voltage ranges 44 and 46 can be used to represent the binary values.

As illustrated in FIG. 3, the high data rate is five times faster than the low data rate. Accordingly, during the same period of time in which three time slots (i.e., T_L=1, 2, 3) of low data rate transmissions elapse, fifteen time slots (i.e., T_H=1, 2, 3, . . ., 15) of high data rate transmissions elapse. This five to one ratio, however, is used only for purposes of illustration; in accordance with the invention, virtually any ratio of the high data rate to the low data rate can be used.

Also as shown in the figure, the data transmitted at the high data rate has a logical value of zero at T_H=1, a logical value of one at T_H=2, a logical value of zero at T_H=3, and so on. These values are transmitted by varying the voltage level on the shared data bus between the low sub-range 54 of the low voltage range 46 and the high sub-range 52 of the low voltage range 46. Then, at time slot T_H=6, the voltage level on the shared data bus 36 is changed from the low voltage range 46 to the high voltage range 44, in accordance with a change in the value of the data bit being transmitted at the low data rate. The high data rate transmission, however, continues on uninterrupted by varying the voltage level between the high sub-range 48 of the high voltage range 44 and the low sub-range 50 of the high voltage range 44. Thus, the high data rate has a logical value of one at T_H=6, a logical value of zero at T_H=7, a logical value of one at T_H=8, and so on. Although the high data rate transmission is shown as alternating between a logical zero and logical one, the voltage level in actual use will not generally follow a set pattern but will depend upon the value to be transmitted at each time slot. Furthermore, although the high data rate transmission is preferably conducted using binary values, data can also be transmitted using more than two values by dividing each low data rate voltage range into a greater number of sub-ranges, wherein each sub-range represents a different value.

In accordance with an alternative embodiment of the invention, the fast data rate transmissions can be made by varying the voltage between different levels of the full voltage swing, while data can be transmitted at a slow data rate by varying the voltage level between sub-levels within each of the full voltage swing levels. In yet another embodiment of the invention, it is possible to use the same data rate for two different data transmissions. In other words, data that is sent using different levels of the full voltage swing can be sent at the same rate as data that is sent using sub-levels within the full voltage swing levels.

Using the present invention, it is possible to implement a slow, simple serial interface and a faster more elaborate interface on a single, shared data bus 36. The simple device 14, for example, can comprise a simple electronics accessory. Little or no modification to the device 14 is necessary to enable it to operate in accordance with the invention because the high data rate traffic on the shared data bus 36 essentially constitutes only a minor, but inconsequential, disturbance on the low data rate transmissions. On the other hand, the electronics for the high-speed device 12 will be more complex because the high-speed device 12 must be capable of detecting and transmitting data signals using at least four different voltage levels. This type of capability, however, will ordinarily be more affordable in more advanced accessories.

Although a preferred embodiment of the method and apparatus of the present invention has been illustrated in the accompanying Drawings and described in the foregoing Detailed Description, it is understood that the invention is not limited to the embodiment disclosed, but is capable of numerous rearrangements, modifications, and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.

What is claimed is:

1. A method for communicating at least two data transfers on a common bus, said method comprising the steps of:

assigning a first value to a first signal range and a different, second value to a separate, second signal range;

transmitting data at a first data rate by varying a signal on the common bus using at least the first signal range and the second signal range;

assigning a value to each of: (i) a first sub-range of the first signal range, (ii) a first sub-range of the second signal range, (iii) a second sub-range of the first signal range, and (iv) a second sub-range of the second signal range; and

transmitting data at a second data rate by varying a signal on the common bus using at least the first sub-range of the first signal range, the first sub-range of the second signal range, the second sub-range of the first signal range, and the second sub-range of the second signal range.

2. The method of claim 1, wherein said first data rate is greater than said second data rate.

3. The method of claim 1, wherein said first data rate is the same as said second data rate.

4. The method of claim 1, wherein said second data rate is greater than said first data rate.

5. The method of claim 4, wherein said first signal range comprises a first range of voltages on the common bus and said second signal range comprises a second range of voltages on the common bus.

6. The method of claim 5, wherein the step of transmitting data at the first data rate comprises transmitting binary data, the first range of voltages representing a logic value zero and the second range of voltages representing a logic value one.

7. The method of claim 6, wherein the first data rate is defined by a plurality of time slots and one binary value is transmitted for each time slot.

8. The method of claim 6, wherein the first sub-range of the first signal range and the second sub-range of the first signal range comprise two distinct subsets within the first range of voltages, and the first sub-range of the second signal range and the second sub-range of the second signal range comprise two distinct subsets within the second range of voltages.

9. The method of claim 8, wherein the step of transmitting data at the second data rate comprises transmitting binary data, the first sub-range of the first range of voltages and the first sub-range of the second range of voltages representing a logic value zero, and the second sub-range of the first range of voltages and the second sub-range of the second range of voltages representing a logic value one.

10. The method of claim 9, wherein the second data rate is defined by a plurality of time slots and one binary value is transmitted for each time slot.

11. The method of claim 10, further comprising the step of concurrently transmitting data at the first data rate and the second data rate.

12. The method of claim 5, wherein the first sub-range of the first signal range and the second sub-range of the first signal range comprise two distinct subsets within the first range of voltages, and the first sub-range of the second

signal range and the second sub-range of the second signal range comprise two distinct subsets within the second range of voltages.

13. The method of claim 12, further comprising the step of concurrently transmitting data at the first data rate and the second data rate.

14. A data communications system, comprising:

a shared data bus;

a first electronic device coupled to the shared data bus for transmitting data via the shared data bus at a first data rate by varying the voltage level on the shared data bus, the first electronic device using at least a voltage level within a first voltage range to represent a first value and a voltage level within a second voltage range, different from the first voltage range, to represent a second value; and

a second electronic device coupled to the shared data bus, the second electronic device communicating data via the shared data bus at a second data rate by varying the voltage level on the shared data bus within the first voltage range when the first electronic device is transmitting the first value and by varying the voltage level on the shared data bus within the second voltage range when the first electronic device is transmitting the second value.

15. The data communications system of claim 14, wherein the second data rate is faster than the first data rate.

16. The data communications system of claim 14, wherein the second data rate is the same as the first data rate.

17. The data communications system of claim 14, wherein the first electronic device comprises a system connector.

18. The data communications system of claim 14, wherein the first electronic device comprises a processor.

19. The data communications system of claim 14, wherein the second electronic device communicates data by varying the voltage level on the shared data bus within the first voltage range between at least a first voltage sub-range representing a third value and a second voltage sub-range representing a fourth value, and by varying the voltage level on the shared data bus within the second voltage range between at least a third voltage sub-range representing the third value and a fourth voltage sub-range representing the fourth value.

20. The data communications system of claim 19, wherein the first value defines a logical zero for communications at the first data rate and the second value defines a logical one for communications at the first data rate.

21. The data communications system of claim 20, wherein the third value defines a logical zero for communications at the second data rate and the fourth value defines a logical one for communications at the second data rate.

22. The data communications system of claim 14, wherein the first electronic device comprises a low-speed device and the second electronic device comprises a high-speed device.

23. A method for communicating at least two data transfers on a common electrical bus, said method comprising the steps of:

transmitting data at a first data rate by varying a voltage on the common electrical bus between at least a first voltage range and a different, second voltage range, wherein said first voltage range represents a first value and the second voltage range represents a second value;

transmitting data at a second data rate by varying a voltage on the common electrical bus between at least a first sub-range of the first voltage range and a second sub-range of the first voltage range when the voltage on the common electrical bus is within the first voltage range, and by varying a voltage on the common electrical bus between a first sub-range of the second voltage range and a second sub-range of the second voltage range when the voltage on the common electrical bus is within the second voltage range, wherein said second data rate is faster than said first data rate.

* * * * *